Amendments to the Specification

Please amend the title as follows:

SYMMETRICAL HIGH FREQUENCY SCR STRUCTURE ~~AND METHOD~~

Please amend the specification paragraphs as follows:

[0011] FIG. 4 illustrates an enlarged cross-sectional view of a prior art SCR ESD structure;

[0018] In general, the present invention provides an SCR device suitable for high frequency (greater than 1 GHz) ESD protection. The SCR device comprises a symmetrical low trigger voltage [[r]] structure. In a preferred embodiment, the structure is integrated into a high frequency bipolar IC process flow, and is isolated from the internal circuitry it protects with a deep isolation trench structure, field dielectrics, and low-doped regions and layers. One can better understand the present invention by referring to FIGS. 1-10 together with the following detailed description of the drawings.

[0026] SCR device 21 has a relatively high trigger voltage V_t on the order of 20 to 25 volts because of low-doped n-well 23 and p-well 24, which typically ~~having~~ have doping levels on the order of 1.0×10^{17} atoms/cm^3. This becomes a problem as IC geometries shrink below 0.8 microns because gate oxide failure voltages become close to the lowest junction breakdown voltage of typical SCR devices. At the 0.8 micron level, worst case gate oxide breakdowns occur in the 10 to 12 volt range, and naturally triggered or typical SCR devices like device 21 require about a 20 to 25

volt transient to turn on. Such a trigger voltage is too high to protect current and future device geometries.

[0029] In addition, control circuits that include series diodes and MOS transistors have been proposed to increase holding voltage over a particular supply bias. Also, control circuits including diodes and grounded gate MOS transistors have been proposed to increase holding current over a particular operating current. Key disadvantages of these proposed solutions include a larger required area on the chip for ESD structure integration, and an increase in the ESD structure's load capacitance, which is directly contrary to the high frequency IC design requirements set forth above.

[0034] According to the present invention, n+ buried layer 413 is maintained floating (i.e., not directly ~~couple~~ coupled to a power rail or ground) to ensure a symmetrical DC breakdown voltage response, and to decrease load capacitance. In addition, n+ buried layer 413 reduces by approximately half the maximum transient voltage bias clamp that results from an ESD event. This allows a very fast and efficient ESD protection, and further reduces required ESD device area on a chip.